IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: **RAYNOR ET AL.**	
Serial No. **10/677,850**	Examiner: **B. SINES**
Filing Date: **October 2, 2003**	Art Unit: **1743**
Confirmation No. **5132**	Attorney Docket No. **03EDI22652634**
For: **METHODS AND APPARATUS FOR SENSOR ALIGNMENT**	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the final Office Action of April 1, 2008, and in connection with the Notice of Appeal filed concurrently herewith, please consider the remarks set out below.

REMARKS

The Applicants believe that the current rejection is primarily based on a lack of understanding by the Examiner of terms commonly used in the electrical engineering field. These terms also relate to "flip-chip technology." The Examiner acknowledged during a telephone interview that he has a chemical background and not an electrical background. In the Amendment After Final filed by the Applicants, several references defining flip-chip technology and other commonly used terms were provided to the Examiner so that he may have a better understanding of such terms. Favorable reconsideration is respectfully requested.

I. The Claims Are Supported By The Specification

The Examiner rejected the claims as including subject matter not supported by the specification. In particular, independent Claims 39 and 57 each recite that the sensor comprises "an integrated circuit die." The Examiner has taken the position that an integrated circuit die is not supported by the specification.

The specification makes reference to a "chip" in paragraphs 11-13. A "chip" is a term for an integrated circuit die. The die, which is a small block of semiconducting material on which a given functional circuit is fabricated, is typically produced in large batches on a single wafer.

The Applicants submit that these terms are readily understood by those skilled in the art. The Applicants thus submit that the specification supports recitation of "integrated circuit die" in the claims.

II. The Claims Are Patentable

The Examiner rejected independent Claims 39 and 57 over the Venkat et al. patent in view of the Bauer et al. patent and in further view of the Casson et al. patent. The Venkat et al. patent discloses an integrated lens and aperture plate for an optical sensor equipped integrated chip in which the lens and the aperture plate are molded as one piece with the lens at the appropriate location so that the lens aligns with the location of the optical sensor. In particular, FIG. 2 in the Venkat et al. patent illustrates a sensor **32** being attached to a mounting substrate **36**. The sensor **32** is attached via the pins extending therefrom by inserting the pins through the openings in the mounting substrate **36**.

As correctly noted by the Examiner, Venkat et al. fails

to disclose the use of bump bonding for attaching the sensor to the mounting substrate. The Examiner cited the Bauer et al. patent, and in particular FIG. 8 therein, as disclosing the use of bump bonding using solder bump **120** in attaching an optical sensor **22** to a mounting base substrate **28** that comprises circuitry (e.g., conductive strip **30**).

In addition, the Examiner cited Casson et al. as disclosing the attachment of a chip device to a flexible printed circuit board using solder bumps to facilitate a secure electrical connection. The Examiner referenced column 16, lines 52-68 as disclosing self-alignment of the chip device to the mounting substrate comprising a flexible printed circuit board using a solder bump bonding methodology that also comprises a heating step.

The Examiner has taken the position that a combination of known elements as disclosed by the cited prior art references would have been obvious to try. The Applicants respectfully disagree, particularly since Venkat et al. simply fails to teach or suggest that the sensor **32** may be mounted in a flip-chip arrangement. Instead, the sensor **32** is a packaged chip or die with a plurality of pins extending therefrom.

A readily understood by those skilled in the art, a "flip chip" is one type of mounting used for semiconductor devices (such as integrated circuit chips), which uses solder bumps instead of wire bonds or pins. In other words, a flip chip arrangement does not require any wire bonds or pins, as disclosed by Venkat et al.

The solder bumps are deposited on the chip pads, located on the top side of the wafer. To mount the chip to external circuitry on a circuit board, it is flipped around, i.e., the top side is facing down towards the mounting area. The

solder bumps are used to connect directly to the associated external circuitry. Even though Venkat et al. discloses that the sensor **32** is mounted face down, it simply fails to teach or suggest that the sensor **32** may be mounted in a flip-chip arrangement in which wire bonds or pins are not required.

The bump bonds in Bauer et al. are attached to a long conductive strip **30** which extends from near the aperture **122** outwards to the edge of the base substrate **28**, as shown in FIG. 8. The same conductive strip is used in all embodiments. It is also clear from FIG. 1 in Bauer et al. that the conductive strip is relatively wide. Bauer et al. is thus silent regarding the issue of alignment.

In Casson et al., the illustrated flip chip **10** fails to disclose a mounting substrate having an opening therethrough as in the claimed invention. Reference is directed to column 7, lines 7-21 of Casson et al. As best illustrated in FIGS. 1a and 1b and as stated above, Casson et al. teaches away from an opening in a mounting substrate associated with the flip chip **10** because of reflow of the soldering between the bonding pads **15** and the solder bumps **16** for providing the electrical connection.

As correctly noted by the Examiner in column 16, lines 52-68 of Casson et al., a solder composition is formed by reflowing solder paste located on the corresponding active contact pad on the circuit board such that a solder bump located on the corresponding bonding pad on the flip chip is allowed to self-align with the corresponding active contact pad and such that the solder paste mixes with the solder bump, and wherein each electrical connection is formed concurrently by applying heat to the circuit board and flip chips as a whole after the flip chips have been placed on the circuit board in a manner which allows for unobstructed motion of the flip chips during

reflow.

If there was an opening in the mounting substrate associated with the flip chip **10** in Casson et al. as in the claimed invention, then the soldering between the bonding pads **15** and solder bumps **17** would not be able to reflow as necessary for providing the desired electrical connection. As noted above, each electrical connection in Casson et al. is formed concurrently by applying heat to the circuit board and to the flip chips **10** as a whole after the flip chips have been placed on the circuit board in a manner which allows for unobstructed motion of the flip chips during reflow.

Accordingly, it is submitted that independent Claims 39 and 57 are patentable over the Venkat et al. patent in view of the Bauer et al. patent and in further view of the Casson et al. patent. In view of the patentability of independent Claims 39 and 57, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

Respectfully submitted,

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